App Note 3558: MAX12557 Schematic and Layout Suggestions

This technical discussion presents proper layout techniques, component selection, and placement for high-speed analog-to-digital converters (ADCs) commonly used in IF and baseband applications. It uses the MAX12557 high-resolution, high-speed data-converter as an example of guidelines that help establish an optimized schematic: proper high-speed layout techniques, bypassing and decoupling tips, component selection and placement, and thermal management guidelines.

Introduction

Maxim's 14-bit dual ADC, the MAX12557, is optimized for a sampling rate of 65Msps and targets all IF and baseband applications. The purpose of this paper is to provide a concise resource for this device's schematic and layout suggestions. It is meant to supplement the schematic and PC-board layout information provided in the component and evaluation board kit data sheets for this ADC. The user should take into consideration his specific application and review all available resources to optimize device performance in the intended application.

This paper is divided into three sections, which are *General Suggestions, Schematic Suggestions*, and *Layout Suggestions.* The *General Suggestions* section offers the user an overview of the design practices that will provide the best overall device performance in his/her application. It mainly discusses best practices in general terms of external component placement around the ADC along with suggestions regarding the physical PC board itself. The *Schematic Suggestions* section provides the user with recommended component values for the most critical and sensitive device pins. Finally, the *Layout Suggestions* section details the component placement recommendations around the converter, identifies which external components should be placed on the top or bottom layer, and finally provides additional information regarding the PC board.

Please refer to **Figure 1** for an illustration of the pinout, and **Table 1** for the MAX12557 pin description. The MAX12557 evaluation (EV) kit includes multiple options to allow for single-ended or differential clock, single-ended or differential analog input, internal/external reference, etc. Therefore, the EV kit schematics in **Figures 2-5** accommodate many more external components and configurations than would be used in a normal application. Finally, **Figures 6** and **7** show silkscreen and component placement for top and bottom layers of the EV kit.
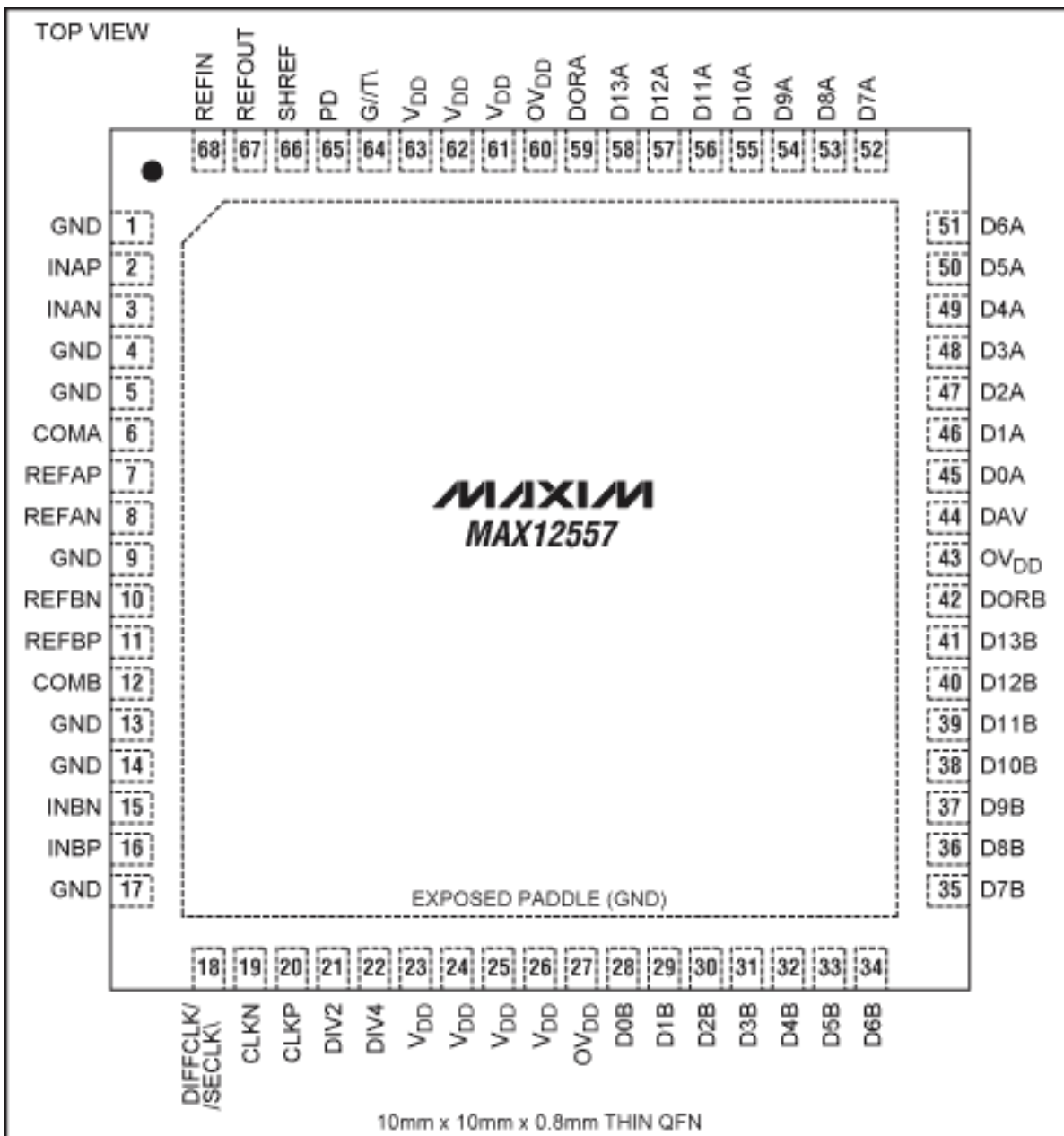
Figure 1. MAX12557 Pinout

Table 1. MAX12557 Pin Description

PIN	NAME	FUNCTION
1, 4, 5, 9, 13, 14, 17	GND	Converter Ground. Connect all ground pins and the exposed paddle (EP) together.
2	INAP	Channel A Positive Analog Input
3	INAN	Channel A Negative Analog Input
6	COMA	Channel A Common-Mode Voltage I/O.
7	REFAP	Channel A Positive Reference I/O. Channel A conversion range is ±2/3 x (V_{REFAP}-V_{REFAN}).

8	REFAN	Channel A Negative Reference I/O. Channel A conversion range is ±2/3 x (V_{REFAP}-V_{REFAN}).
10	REFBN	Channel B Negative Reference I/O. Channel B conversion range is ±2/3 x (V_{REFBP}-V_{REFBN}).
11	REFBP	Channel B Positive Reference I/O. Channel B conversion range is ±2/3 x (V_{REFBP}-V_{REFBN}).
12	COMB	Channel A Common-Mode Voltage I/O
15	INBN	Channel B Negative Analog Input
16	INBP	Channel B Positive Analog Input
18	DIFFCLK//SECLK\	Differential/Single-Ended Input Clock Drive. This input selects between single-ended or differential clock input drives. DIFFCLK//SECLK\ = GND: Selects single-ended clock input drive. DIFFCLK//SECLK\ = OV_{DD}: Selects differential clock input drive.
19	CLKN	Negative Clock Input. In differential clock input mode (DIFFCLK//SECLK\ = OV_{DD} or V_{DD}), connect a differential clock signal between CLKP and CLKN. In single-ended clock mode (DIFFCLK//SECLK\ = GND), apply the clock signal to CLKP and tie CLKN to GND.
20	CLKP	Positive Clock Input. In differential clock input mode (DIFFCLK//SECLK\ = OV_{DD} or V_{DD}), connect a differential clock signal between CLKP and CLKN. In single-ended clock mode (DIFFCLK//SECLK\ = GND), apply the single-ended clock signal to CLKP and connect CLKN to GND.
21	DIV2	Divide-by-Two Clock Divider Digital Control Input
22	DIV4	Divide-by-Four Clock Divider Digital Control Input
23-26, 61, 62, 63	V_{DD}	Analog Power Input. Connect V_{DD} to a 3.15V to 3.60V power supply. Connect all V_{DD} pins to the same potential.
27, 43, 60	OV_{DD}	Output Driver Power Input. Connect OV_{DD} to a 1.7V to V_{DD} power supply.
28, 29, 45, 46	N.C.	No Connect
30	D0B	Channel B CMOS Digital Output, Bit 0 (LSB)
31	D1B	Channel B CMOS Digital Output, Bit 1
32	D2B	Channel B CMOS Digital Output, Bit 2
33	D3B	Channel B CMOS Digital Output, Bit 3
34	D4B	Channel B CMOS Digital Output, Bit 4
35	D5B	Channel B CMOS Digital Output, Bit 5

36	D6B	Channel B CMOS Digital Output, Bit 6
37	D7B	Channel B CMOS Digital Output, Bit 7
38	D8B	Channel B CMOS Digital Output, Bit 8
39	D9B	Channel B CMOS Digital Output, Bit 9
40	D10B	Channel B CMOS Digital Output, Bit 10
41	D13B	Channel B CMOS Digital Output, Bit 11 (MSB)
42	DORB	Channel B Data Out-of-Range Indicator. The DORB digital output indicates when the channel B analog input voltage is out of range. DORB = 1: Digital outputs exceed full-scale range. DORB = 0: Digital outputs are within full-scale range.
44	DAV	Data Valid Digital Output. The rising edge of DAV indicates that data is present on the digital outputs. The evaluation kit utilizes DAV to latch data into external back-end digital logic.
47	D0A	Channel A CMOS Digital Output, Bit 0 (LSB)
48	D1A	Channel A CMOS Digital Output, Bit 1
49	D2A	Channel A CMOS Digital Output, Bit 2
50	D3A	Channel A CMOS Digital Output, Bit 3
51	D4A	Channel A CMOS Digital Output, Bit 4
52	D5A	Channel A CMOS Digital Output, Bit 5
53	D6A	Channel A CMOS Digital Output, Bit 6
54	D7A	Channel A CMOS Digital Output, Bit 7
55	D8A	Channel A CMOS Digital Output, Bit 8
56	D9A	Channel A CMOS Digital Output, Bit 9
57	D10A	Channel A CMOS Digital Output, Bit 10
58	D13A	Channel A CMOS Digital Output, Bit 11 (MSB)
59	DORA	Channel A Data Out-of-Range Indicator. The DORA digital output indicates when the channel A analog input voltage is out of range. DORA = 1: Digital outputs exceed full-scale range. DORA = 0: Digital outputs are within full-scale range.
64	G//T\	Output Format Select Digital Input. G//T\ = GND: Two's complement output format selected. G//T\ = OV_{DD}: Gray code output format selected.
65	PD	Power Down Digital Input. PD = GND: ADCs are fully operational. PD = OV_{DD}: ADCs are powered down.

66	SHREF	Shared Reference Digital Input. SHREF = V_{DD}: Shared Reference Enabled SHREF = GND: Shared Reference Disabled When sharing the reference, externally connect REFAP and REFBP together to ensure that V_{REFAP} equals V_{REFBP}. Similarly, when sharing the reference, externally connect REFAN to REFBN together to ensure that VREFAN = VREFBN.
67	REFOUT	Internal Reference Voltage Output. The REFOUT output voltage is 2.048V. For internal reference operation, connect REFOUT directly to REFIN or use a resistive divider from REFOUT to set the voltage at REFIN. For external reference operation, REFOUT is not required and must be bypassed to GND with a $\geq 0.1\mu F$ capacitor.
68	REFIN	Single-Ended Reference Analog Input. For internal reference and buffered external reference operation, apply a 0.7V to 2.3V DC reference voltage to REFIN. For unbuffered external reference operation, connect REFIN to GND. In this mode REF_P, REF_N, and COM_ are high impedance inputs that accept the external reference voltages.
-	EP	Exposed Paddle. EP is internally connected to GND. Externally connect EP to GND to achieve specified dynamic performance.

General Suggestions

- In general, multilayer boards with solid ground planes and power planes produce the highest level of signal integrity.
- The MAX12557 requires high-speed board layout design techniques, including a solid ground-plane connection to the exposed paddle.
- Keep the inner-layer ground-plane integrity on the analog side of the MAX12557 extremely solid, with absolute minimum voids. Stagger vias by using very small via clearances to minimize voids. Also, keep a solid ground beneath the critical components, especially the REFAP, REFAN capacitors on pins 7 and 8; the pin 6 COMA bypass; REFBP, REFBN capacitors on pins 11 and 10; the pin 6 and 12 COMB bypass; and the small-valued capacitors around the analog A input pins 2 and 3 and the analog B input pins 15 and 16.
- Confine the different input and output signals to well-defined layer locations, all analog inputs in layer X, all digital outputs on layer Y, all clocks on layer Z, etc. Try to trap each layer between two solid ground planes or as microstrip.
- Use power-supply planes instead of ground traces to minimize inductance for these signals and to minimize overall noise. If power traces are used, they should be made physically wide to minimize IR drop and inductance.
- For GND and V_{DD} (power connections), Maxim recommends multiple vias with 18-mil drill size.

- All MAX12557 GNDs and the exposed paddle (EP) must be connected to the same ground plane. The MAX12557 relies on the EP connection for a low-inductance ground connection using multiple vias to the designated ground layer. The number of vias required depends on the via-hole size. As a guideline, Maxim suggests using a matrix of 5 x 5 (25 total) 13-mil vias. A minimum of 12 vias is required to ensure adequate ground connection.
- The most critical connections in and out of the MAX12557 are analog input, reference pins, clock, and the digital output traces. The most critical pins are 2, 3, 6-8, 10-12, 15, 16, 19, 20, 67, and 68.
- Traces connecting bypass and critical capacitors around the ADC should be as wide as possible to minimize resistance and inductance. Trace widths greater than or equal to 10mils are recommended. Ground traces should be made as wide as possible if the component is not located directly above the ground plane. This includes any ground thermals used in PC-board designs.
- If thermals are used to route a bypass capacitor to GND, use two thermals per capacitor with a via at the GND end of each thermal to minimize inductance.
- Route high-speed digital signal traces away from the sensitive analog traces, clock traces, and REFP, REFN.
- Keep all signal lines (including REFP, REFN) short and free of 90° turns.
- Ensure that the differential analog-input network layout is symmetrical and that all parasitics are balanced equally.
- Position all bypass capacitors as close to the ADC as possible, preferably on the same side of the PC board as the converter using surface-mount devices to limit the inductance (described in greater detail in *Layout Suggestions* section).
- In general, all GND bypass vias should have a drill size of 18 mils.
- This ADC requires separate analog and digital power supplies for best performance.
- The MAX12557 allows for either differential or single-ended signals to the clock inputs.
- The MAX12557 accepts differential or single-ended analog input signals. Differential signals provide optimum performance.
- The converter's EP acts as the main ground for the device and therefore MUST be properly attached to the designated ground plane.
- Use a ground "island" between the ADC circuit and any other adjacent circuitry that might be included on the board. For example, if multiple ADCs are used on a single board, separate their associated circuits by placing a ground plane between them.

Schematic Suggestions (Figures 2-5)

- (Pins 2 and 3, INAP and INAN): Depending on the application, to achieve best overall AC performance, shunt capacitors should be included on these pins-to-ground having a value ranging from 5.6pF to 12pF. These capacitor values can be included in the resonant circuit of any anti-aliasing filter driving the ADC and should be located on the top of the board.
- (Pin 6, COMA): Bypass COMA to GND with a good, high-frequency 2.2µF ceramic capacitor.
- (Pin 7, REFAP): Bypass REFAP to GND with a high-frequency (up to 1.0µF) ceramic capacitor on the top side of the board. Keep all REFAP traces short.
- (Pin 8, REFAN): Bypass REFAN to GND with a high-frequency (up to 1.0µF) ceramic capacitor on the top side of the board. Keep all REFAN traces short.
- (Pin 10, REFBN): Bypass REFBN to GND with a high-frequency (up to 1.0µF) ceramic

capacitor on the top side of the board. Keep all REFBN traces short.

- (Pin 11, REFBP): Bypass REFBP to GND with a high-frequency (up to 1.0µF) ceramic capacitor on the top side of the board. Keep all REFBP traces short.
- (Pin 12, COMB): Bypass COMB to GND with a good, high-frequency 2.2µF ceramic capacitor.
- (Pins 15 and 16, INBN and INBP): To achieve best overall AC performance, shunt capacitors should be included on these pins-to-ground having a value ranging from 5.6pF to 12pF, depending on the application. These capacitor values can be included in the resonant circuit of any anti-aliasing filter driving the ADC and should be located on the top of the board.
- (Pins 23-26, 61-63, V_{DD}): Bypass V_{DD} to GND with a good, high-frequency 0.1µF ceramic capacitor in parallel with a good, high-frequency $\geq$2.2µF ceramic capacitor.
- (Pins 27, 43, 60, OV_{DD}): Bypass OV_{DD} to GND with a good, high-frequency 0.1µF ceramic capacitor in parallel with a good, high-frequency $\geq$2.2µF ceramic capacitor.
- (Pins 28-41, D0B-D13B): Include series resistors from the data-output pins to their respective load. These resistors limit the high-frequency edge current into the internal chip GND from the output-logic drivers. Choose a value that, when combined with the load capacitance, will yield an RC time constant of approximately 1ns. Maxim uses a very small and inexpensive resistor array, such as the Panasonic EXB-2HV-221J (refer to MAX12557 EV kit bill of materials list).
- (Pins 45-58, D0A-D13A): Include series resistors from the data-output pins to their respective load. These resistors limit the high-frequency edge current into the internal chip GND from the output-logic drivers. Choose a value that, when combined with the load capacitance, will yield an RC time constant of approximately 1ns. Maxim uses a very small and inexpensive resistor array, such as the Panasonic EXB-2HV-221J (refer to MAX12557 EV kit bill of materials list).
- Internal Reference-Voltage Output (pin 67, REFOUT): The REFOUT voltage is 2.048V and REFOUT can deliver 1mA. For internal reference operation, connect REFOUT directly to REFIN or use a resistive divider from REFOUT to set the voltage at REFIN. Bypass REFOUT to GND with a good, high-frequency $\geq$0.1µF ceramic capacitor.
- Single-Ended Reference Analog Input (pin 68, REFIN): For internal reference and buffered external reference operation, apply a 0.7V to 2.3V DC reference voltage to REFIN. Within its specified operating voltage, REFIN has a >50MΩ input impedance, and the differential reference voltage ($V_{REF\_P} - V_{REF\_N}$) is generated from REFIN. In the internal reference mode and buffered external reference mode, bypass REFIN to GND with a good, high-frequency $\geq$0.1µF ceramic capacitor. For unbuffered external reference-mode operation, connect REFIN to GND.
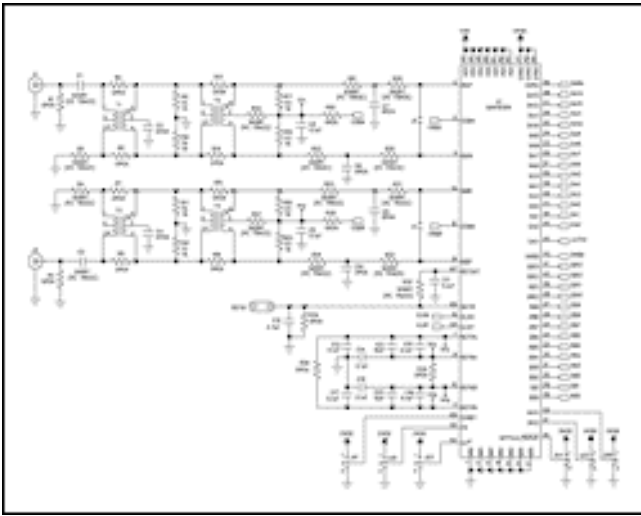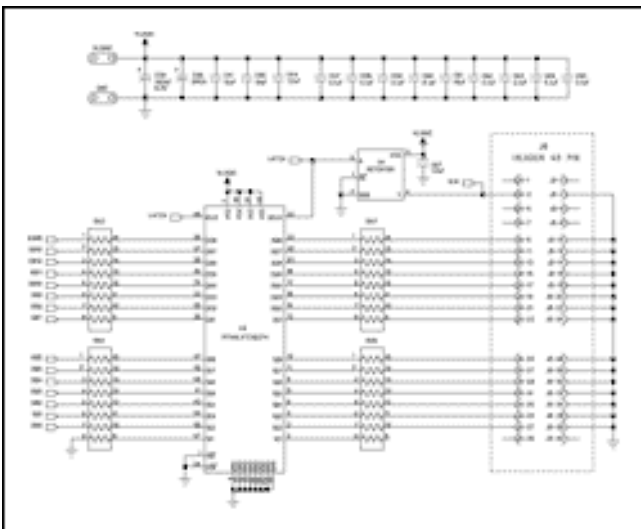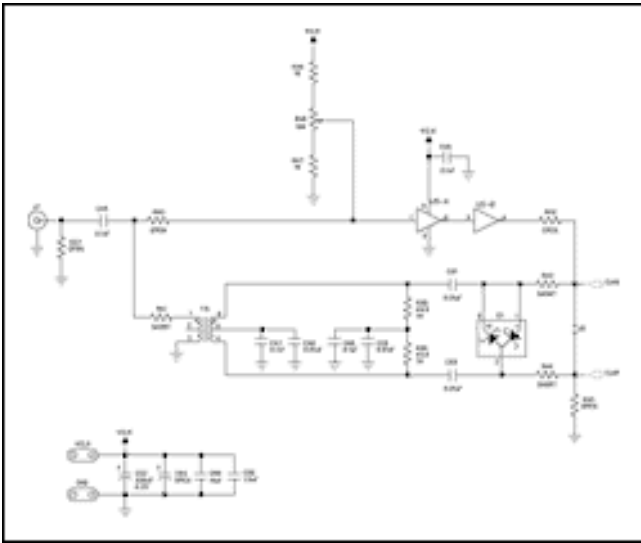
Figure 2. MAX12557 EV Kit Analog-Input Section Schematic
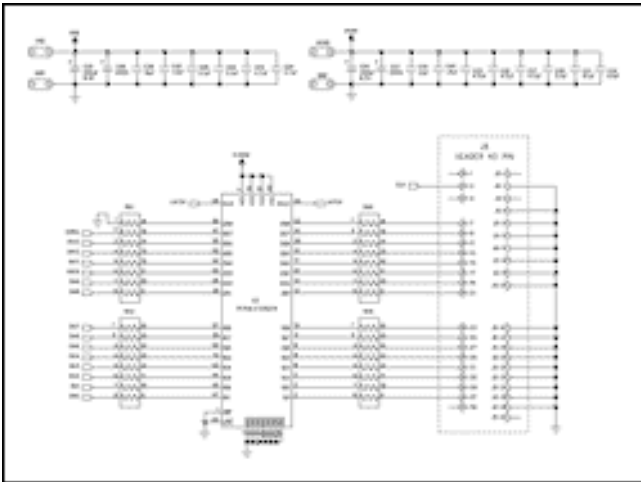
Figure 3. MAX12557 EV Kit Digital A Output Schematic

Figure 4. MAX12557 EV Kit Digital B Output Schematic

Figure 5. MAX12557 EV Kit Clock Circuitry

Layout Suggestions (See Figures 6 and 7 for Critical Component Placement)
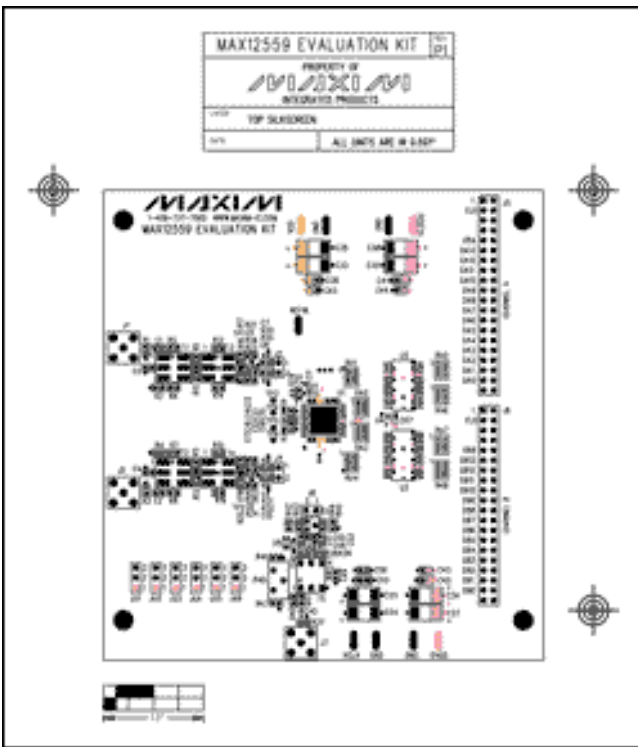
- Place the MAX12557 on the top side of the PC board.
- All converter GND pins (1, 4, 5, 9, 13, 14, and 17) should be physically routed to the copper beneath the MAX12557 using traces.
- The analog input circuit for each converter should be balanced; that is, the trace lengths from the driving source (amplifier, filter, etc.) to the differential inputs should be the same length, and the placement of the components should be symmetrical to one another so that all parasitics are equally balanced. These lines should be kept short to minimize inductance and avoid noise and signal pickup from other sections of the board.
- Minimize the shunt capacitor trace lengths on the analog-input pins 2 and 3 (INAP and INAN) by placing them close to the device pins on the top of the board.
- Next, place the 2.2µF capacitor from pin 6 (COMA) to GND as close as possible to the device. This capacitor can be located on the bottom of the board and connected to pin 6 using a 13-mil via, if needed. The trace should be kept short.
- Next, place the 1µF capacitor between pins 7 and 8. This capacitor should be located on the top side of the board as close to these pins as possible. The 1µF cap across REFAP and REFAN (pins 7 and 8) should be as close to the DUT as manufacturing tolerances allow.
- Next, place the bypass capacitors from pin 7 to ground and from pin 8 to ground. These capacitors should be placed next to the shared 1µF capacitor as close as possible, and vias should be used to connect the GND end of these capacitors to the designated analog ground layer (also connected to the device EP). If there is a ground plane on layer two, this plane should extend under these three components to reduce the inductance to pins 1 and 2. For the REFAP and REFAN ground vias, Maxim uses a drill diameter of 18 mils, which has been oversized by 3 mils to account for plating. The final via-hole size should look more like 15 mils.
- Next, place the 10µF capacitor between pins 7 and 8. If sufficient space is not available on the top layer for this capacitor, it can be included on the bottom of the board using vias to route the signals, as is done on the EV kit. Minimize the overall trace lengths connecting this capacitor to the device pins

- Next, place the 1µF capacitor between pins 10 and 11. This capacitor should be located on the top side of the board as close to these pins as possible. The 1µF cap across REFBN and REFBP (pins 10 and 11) should be as close to the converter as manufacturing tolerances allow.
- Next, place the bypass capacitors from pin 10 to ground and from pin 11 to ground. These capacitors should be placed next to the shared 1µF capacitor as close as possible, and vias should be used to connect the GND end of these capacitors to the designated analog ground layer (also connected to the device EP). If there is a ground plane on layer two, this plane should extend under these three components to reduce the inductance to pins 1 and 2. For the REFBP and REFBN ground vias, Maxim uses a drill diameter of 18 mils, which has been oversized by 3 mils to account for plating. The final via-hole size should look more like 15 mils.
- Next, place the 10µF capacitor between pins 10 and 11. If sufficient space is not available on the top layer for this capacitor, it can be included on the bottom of the board using vias to route the signals, as is done on the EV kit. Minimize the overall trace lengths connecting this capacitor to the device pins.
- The trace lengths to and from pins 7 and 8 should be short in length and should be matched; that is, they should be symmetrical and the same length.
- The trace lengths to and from pins 10 and 11 should be short in length and should be matched; that is, they should be symmetrical and the same length.
- Next, place the 2.2µF capacitor from pin 6 (COMB) to GND as close as possible to the device. This capacitor can be located on the bottom of the board and connected to pin 6 using a 13-mil via if needed. The trace should be kept short.
- Minimize the shunt-capacitor trace lengths on the analog-input pins 15 and 16 (INBN and INBP) by placing them close to the device pins on the top of the board.
- It is imperative that the MAX12557 EP be properly connected to the designated ground plane (preferable layer 2). This can only be accomplished using a sufficient number of vias to minimize inductance, with the number dependent on the hole size. As a guideline, Maxim recommends a matrix of 5 x 5 (25 total) 13-mil vias be used; a minimum of 12 is required.
- A single layer (preferably layer 2) should be used as solid analog ground to which the MAX12557 EP is connected using the recommended via array.
- Clock suggestions (pins 19 and 20): The clock inputs are at least as sensitive as the analog inputs and reference pins. Treat the clock lines the same as you would the analog signal lines. Avoid running the clock lines close to any digital-output signals. If multiple ADCs are used on one board, separate clock line pairs to minimize noise and signal pickup from other ADC sections. Clock signals should not be on the same layer as the data-output lines. If they are, attempt to eliminate any coupling that might occur by keeping a relatively large physical distance between the two signal types and by routing GND between the two signal types.

  For a differential clock input, we recommend a typical value of 1.4VP-P because that is what is used to characterize this converter. However, it is not the peak-to-peak input-clock signal swing that is the most important, but rather the slew-rate-to-yield fast rise and fall times. Also, an internal differential amplifier provides gain and further squares-up the signal. On the EV kit, we step-up the clock input using a center-tapped transformer to ensure fast rise and fall times, and then limit the amplitude to 1.4VP-P using diodes. For a single-ended clock, the edges should be sharp, having the maximum and minimum voltages specified in the

datasheet as $0.8V_{DD}$ (min) for the high logic level and $0.2V_{DD}$ (max) for the low logic level. The clock common-mode voltage ($1/2V_{DD}$) is generated internally. Recommended interface circuit/driver logic: Any of the logic families, including input CMOS, LVPECL, and LVDS, can be used for driving the clock input. For the most demanding applications with high-frequency input signals, very high-speed LVPECL clock distribution is recommended, such as the MAX9320 PECL buffer.

- (Pins 23-26, 61-63, V_{DD}): Best practice is to locate the 0.1µF bypass capacitor right next to the device pins.
- (Pins 27, 43, 60, OV_{DD}): Best practice is to locate the 0.1µF bypass capacitor right next to the device pins.
- Data Lines B (pins 28-41) and Data Lines A (pins 44-58): For the output-data pins, try to keep the traces from the ADC to the buffer or load IC short. Place the series resistors very close to the ADC and target a total load capacitance of $\geq$10pF to ensure optimal performance. It is very important that the buffer or load IC has a solid ground plane back to the MAX12557 EP ground to achieve optimum AC performance. If the data lines are routed on the top or bottom layer (microstrip technique), the adjacent layer should always be a ground plane to form effective transmission lines. If the data lines are routed through an inner layer (stripline technique), both adjacent layers must be at ground potential to form an effective transmission line. Confine the digital-signal outputs to be tightly arranged in a single bus to control the return current path. Also, minimize the ground-plane voids (created by digital-signal vias) between the MAX12557 and digital load, perhaps through staggering the via arrangement when the data lines are dropped to an inner layer.
- Shared Reference (pin 66, SHREF): When sharing the reference, externally connect REFAP and REFBP together to ensure that $V_{REFAP} = V_{REFBP}$. Similarly, when sharing the reference, externally connect REFAN to REFBN together to ensure that $V_{REFAP} = V_{REFBP}$.
- Bypass capacitors to REFOUT and REFIN (pins 67 and 68) must be located close to the device pins using short traces and grounded directly to the device ground plane.

Figure 6. MAX12557 EV Kit Top Side Silkscreen and Component Placement
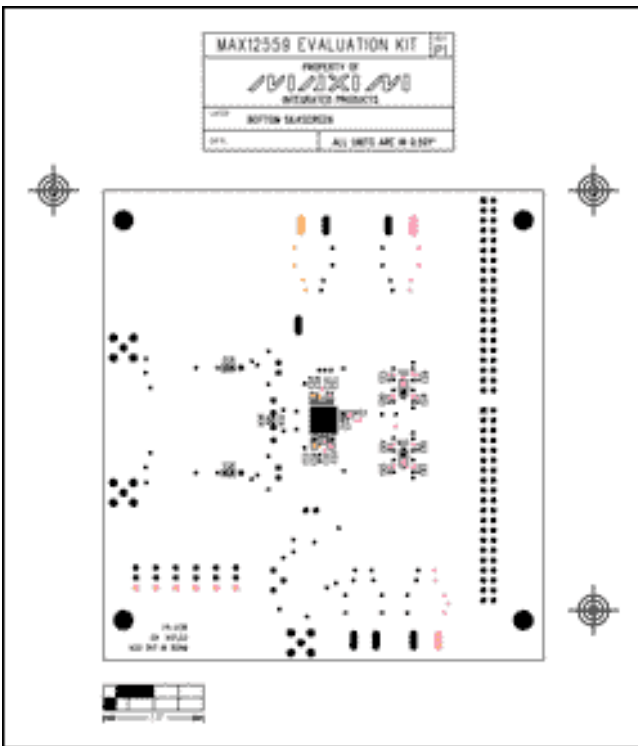
Figure 7. MAX12557 EV Kit Bottom Side Silkscreen and Component Placement

Conclusion

If the user follows the suggestions provided in this application note to supplement information in the device and EV kit data sheets, device performance will be optimized in the intended application.

More Information

MAX12527: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX12528: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX12557: QuickView -- Full (PDF) Data Sheet -- Free Samples